REMARKS

In the Office Action, the Examiner indicated that claims 1-14 are pending and that claims 1-14 are rejected. By this response, claim 1 is amended. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. REJECTION OF CLAIMS 1-3, 5, 6, 9, 10 AND 13 UNDER 35 U.S.C. § 102

The Examiner rejected claims 1-3, 5, 6, 9, 10 and 13 as being anticipated under 35 U.S.C. § 102 by US Patent 6,599,831, issued on July 29, 2003, hereinafter referred to as "Maszara." The Applicants respectfully traverse the rejection.

Maszara teaches a metal gate electrode using silicidation and method of formation thereof. Maszara teaches forming a dielectric on a substrate, followed by forming and doping a polysilicon body on the dielectric. (See Maszara, col. 2, ll. 59-67). Next a metal layer, for example nickel, is deposited over the polysilicon body and silicided. (See Maszara, col. 3, ll. 29-51). The silicidation process creates a higher dopant concentration on the portion of the gate adjacent the gate oxide than the gate portion further away from the gate oxide. (See Maszara, col. 3, l. 59 – col. 4, l. 16).

Maszara, however, fails to teach each and every element of Applicants' invention recited in amended claim 1. Namely, Maszara does not teach or suggest forming a gate structure having raised source and drain regions. Specifically, Applicants' amended claim 1 positively recites:

> A method of fabricating a complementary metal oxide semiconductor (CMOS) field effect transistor, comprising the steps of:
>
> (a) providing a substrate;
>
> (b) providing on said substrate a polysilicon layer formed upon a gate dielectric layer;
>
> (c) doping the polysilicon layer using at least one dopant;
>
> (d) forming a gate structure for the transistor having a polysilicon gate electrode and raised source and drain regions;
>
> (e) depositing on the polysilicon gate electrode at least one of a metal and an alloy; and

(f) siliciding the polysilicon gate electrode to form a silicide and at least one monolayer of the at least one dopant at an interface between the gate dielectric layer and the silicide.

(Emphasis added). In contrast, Maszara discloses source and drain regions formed in the substrate (see Maszara, FIG. 5, elements 56 and 58). Maszara is devoid of any teaching or suggestion of forming a gate structure having raised source and drain regions. Accordingly, Maszara does not anticipate Applicants' invention of amended claim 1.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Maszara does not teach or suggest forming a gate structure having raised source and drain regions, Maszara does not teach each and every element of Applicants' claim 1. Moreover, dependent claims 2-3, 5-6, 9-10, and 13 depend, either directly or indirectly, from independent claim 1 and recite additional features. As such, and for the exact same reason set forth above, the Applicants submit that 2-3, 5-6, 9-10, and 13 are also not anticipated and allowable.

Therefore, Applicants contend that claims 1-3, 5-6, 9-10, and 13 are patentable over Maszara and, as such, fully satisfy the requirements of 35 U.S.C. §102. Thus, Applicants respectfully request that the rejection of such claims be withdrawn.

II. REJECTION OF CLAIMS 4, 7, 8, 11, 12 AND 14 UNDER 35 U.S.C. §103

A. Claim 4

The Examiner rejected claim 4 as being unpatentable under 35 U.S.C. § 103 over Maszara in view of U.S. Patent 6,518,113, issued February 11, 2003, hereinafter referred to as "Buynoski." The Applicants respectfully traverse the rejection.

The teachings of Maszara are discussed above. Buynoski teaches doping of thin amorphous silicon work function control layers of MOS gate electrodes. Buynoski's method applies to in-laid ("damascene") gates. (See Buynoski, Col. 1, Lines13-15.) Both methods taught by Buynoski involve forming the source drain regions, forming a doped polysilicon layer over a thin gate insulator layer and then filling a void with a

metal contact (i.e. the "damascene" method). (See Buynoski, Fig. 7(A), Fig. 16(A); Col. 12, Line 43 - Col. 13, Line 21.)

Claim 4 depends from claim 1 and recites additional features therefor. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 1. Namely, the combination of Maszara and Buynoski does not teach or suggest forming a gate structure having raised source and drain regions. As discussed above, Maszara does not teach or suggest raised source and drain regions. Buynoski is likewise devoid of any teaching or suggestion of raised source and drain regions. Rather, the source and drain regions in Buynoski are formed in the substrate (see Buynoski, FIG. 4, elements 26 and 28). Since neither Maszara nor Buynoski teach or suggest forming a gate structure having raised source and drain regions, no conceivable combination of Maszara and Buynoski renders obvious Applicants' invention in claim 1. Therefore, Applicants contend that claim 4, which depends from claim 1, is patentable over the cited combination and, as such, fully satisfies the requirements of 35 U.S.C. §103. Accordingly, Applicants respectfully request that the rejection of claim 4 be withdrawn.

B. Claims 7, 8, 11, 12 and 14

The Examiner rejected claims 7, 8, 11, 12 and 14 as being unpatentable under 35 U.S.C. § 103 over Maszara in view of U.S. Patent 6,624,489, issued September 23, 2003, hereinafter referred to as "Chong." The Applicants respectfully traverse the rejection.

The teachings of Maszara are discussed above. Chong teaches formation of silicided shallow junctions using implant through metal technology and laser annealing process. The method taught by Chong forms a gate transistor comprising a silicide layer, heavily doped layer, polysilicon layer, and a gate oxide layer, in that order. (See Chong, Fig. 11, Col. 5, Line 44 - Col. 6, Line 15.)

Claims 7-8, 11-12, and 14 depend from claim 1 and recite additional features therefor. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 1. Namely, the combination of Maszara and Chong does not teach or suggest forming a

gate structure having raised source and drain regions. As discussed above, Maszara does not teach or suggest raised source and drain regions. Chong is likewise devoid of any teaching or suggestion of raised source and drain regions. Rather, the source and drain regions in Chongi are formed in the substrate (see Chong, FIG. 3, element 14). Since neither Maszara nor Chong teach or suggest forming a gate structure having raised source and drain regions, no conceivable combination of Maszara and Chong renders obvious Applicants' invention in claim 1. Therefore, Applicants contend that claims 7-8, 11-12, and 14, which depend from claim 1, are patentable over the cited combination and, as such, fully satisfy the requirements of 35 U.S.C. §103. Accordingly, Applicants respectfully request that the rejection of claims 7-8, 11-12, and 14 be withdrawn.

Conclusion

Thus, the Applicants submit that all of these claims now fully satisfy the requirements of 35 U.S.C. §§ 102 and 103. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring the maintenance of any final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Kin-Wah Tong, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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